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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,452	09/10/2003	Thane M. Larson	10008321-2	4904

7590 01/26/2007

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EXAMINER	
DINH, TUAN T	
ART UNIT	PAPER NUMBER
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,452	LARSON, THANE M.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20 and 30-33* is/are pending in the application.

4a) Of the above claim(s) *30-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20,33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Noted of claim language:

Claim 13, lines 15-17, recites "said second electrical contact area on said second side of said substrate ***is used for*** IC testing" is not positive claim language because the term "***used for***" which shows a *functional language and intended use* for the second contact area. Further, "the capacitor plate is connected to said second contact area of a substrate or board ***after IC testing***" is inherently and well known in the art because the contact area (contact test or wiring or pattern) would be test first to make sure the contact test area has an electrical conductivity while components mounted on the substrate or board, so if the capacitor plate is connected to the contact area before the test that cause breaking pins on the test machine.

For claim 13, line 18, the term "selected capacitance value" of the capacitor is known in art of the electronic component. The capacitor is inherently having a value capacitance verified on a surface of the capacitor.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 13, lines 20-21, it is unclear. The phrase of "***the selected capacitance value is based on an electrical model of the capacitor plate and on a verification of the capacitance value***" is not understood. What does applicant mean? What does applicant means of "an electrical model". Does applicant mean that term means the capacitor having a value of capacitance based on its model (for example, 1, 2, ...100nF on a top surface of the capacitor)?

By applying art, the examiner assumes that that phrase should be read as "***the selected capacitance value is based on a model of the capacitor plate and on a verification of the capacitor plate"***.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 13, 16, 18-20 rejected under 35 U.S.C. 102(b) as being anticipated by Jodoin (U.S. Patent 4,636,918) submitted by applicant.

As to claims 13, 16-17, Jodoin discloses an assembled substrate, which is a PCB having a LGA, as shown in figures 5-6 comprising:

a substrate (14,column 4, line 44) having first and second sides (top and bottom surfaces-34, 36, column 4, lines 48, 51), and

first and second electrical contact areas (PTH-16 and conductors or traces 18) formed on said first and second sides (34, 36) and separated by an insulating or dielectric material of the substrate (14);

an electrical component (10) having a plurality of leads (12) *electrically connected* to said first electrical contact area of said substrate (14), (noted: leads 12 of an IC 10 electrically connected to the traces 18); and

a capacitor plate (20, column 4, line 49) *electrically connected* to said second electrical contact area on said second side (36) of said substrate (14) substantially opposite said first electrical contact area of said substrate and is ***used for*** (intended use) in-circuit (IC) testing.

The capacitor plate (20) inherently having a selected value (the value has been selected by the manufacturing whom made the capacitor (vender)) that also based on a model (the vender name) and verified the value on the surface of the capacitor.

As to claim 18, Jodoin discloses said capacitor plate (20) having a plurality of layers of dielectric material (30-figure 6) separating a plurality layers of conductive material (24, 26), see column 4, lines 7-9.

As to claim 19, Jodoin discloses said capacitor plate (20) comprises: a plurality of conductive power and ground planes (24, 26), wherein said plurality of conductive

power and ground planes are separated by one or more dielectric layers (30) including a dielectric layer chosen from a ceramic.

As to claim 20, Jodoin discloses said capacitor plate (20) is attached by solder to said second electrical contact area on said second side of said substrate (14) (it is inherently to feed the pins/leads of the capacitor plate into PTH (16) by applying solder for electrical connection).

5. Claims 13, 16-20, 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozak et al. (U.S. Patent 6,414,850) submitted by applicant.

As to claims 13, 16-17, Kozak et al. discloses an assembled substrate, which is a PCB, as shown in figures 1-7 comprising:

a substrate (114) having first and second sides (top and bottom surfaces), and first and second electrical contact areas (134) on said first and second sides;

an electrical component (112), which is a BGA device (column 4, line 26) having a plurality of leads (ball pads underneath of the chip 112) electrically connected to said first electrical contact area of said substrate (114); and

a capacitor plate (412, column 4, lines 33-34) electrically connected to said second electrical contact area on said second side of said substrate (114) substantially opposite said first electrical contact area of said substrate and is used for (intended use) in-circuit (IC) testing.

The capacitor plate (412) inherently having a selected value (the value has been selected by the manufacturing whom made the capacitor (vender)) that also based on a

model (the vender name) and verified the value on the surface of the capacitor. Further on column 4, lines 37-40 of Kozak et al that disclose the selected capacitance value of the capacitor depended on layers laminated on. Thus, the capacitor plate (412) having a selected value.

As to claim 18, Kozak et al. discloses said capacitor plate (412) having a plurality of layers of dielectric material (618a-e-figure 6) separating a plurality layers of conductive material (612a-c and 614a-c, see figure 6), see column 4, lines 55-59.

As to claim 19, Kozak discloses said capacitor plate (412) comprises: a plurality of conductive power and ground planes (614, 612), wherein said plurality of conductive power and ground planes are separated by one or more dielectric layers (618) including a dielectric layer chosen from a ceramic.

As to claim 20, Kozak discloses said capacitor plate (412) is attached by solder to said second electrical contact area on said second side of said substrate (114).

As to claim 33, Kozak et al. disclose the capacitor (412) having a model (vender name) that created by a computer aided design software (for example, print a label that verify the name and value of the capacitor).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozak et al. ('850) or Jodoin ('918) in view of Kabadi (U.S. Patent 6,097,609), and further in view of Wisser (U.S. patent 3,721,941).

As to claim 14, Kozak or Jodoin disclose all of the limitations of the claimed invention, except for a first interposer (or socket) between said component and said first electrical contact area on said first side of said substrate; and a second interposer (or socket) between said capacitor plate and said second electrical contact area on said second side of said substrate.

Kabadi teaches a dual socket for two components (320, 360-fgure 4), and further Wisser shows a multiple socket with pins feeding through a PCB (21, see figures 1-2).

Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to have teaching of Kobadi and Wisser employ in the substrate of Kozak et al. or Jodoin in order to perform interconnections between components on board without any manner damage.

Response to Arguments

Applicant's arguments with respect to claims 13-20 and 30-32 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues:

Either Jodoin or Kozak does not or silent regarding a selected capacitance value.

Examiner disagrees because the capacitor plate inherently having a selected value (the value has been selected by the manufacturing whom made the capacitor

(vender)) that also based on a model (the vender name) and verified the value on the surface of the capacitor.

Therefore, the examiner believes the Office action is proper.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
January 16, 2007.